BEE 271 Digital circuits and systems
Spring 2017 Lab rubric

Instructor Nicole Hamilton
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Office hours TBD and by appointment
(I do not have an on-campus office.)

Grader Austen Szypula
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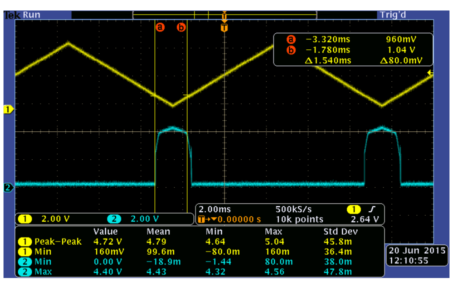
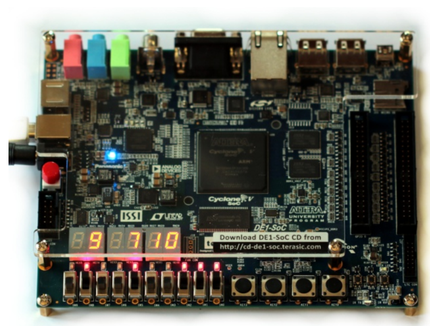
Lab Mondays, 3:30 to 5:30 pm
Beardslee 220

Organization

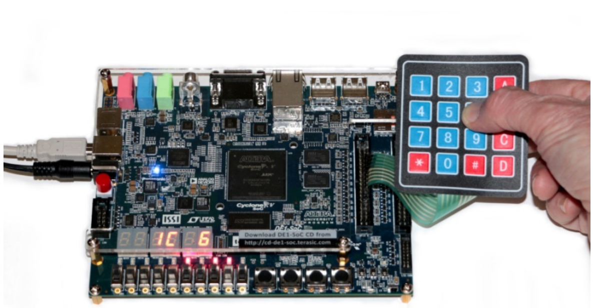
This laboratory is organized as a series of four assignments due at roughly two week intervals.



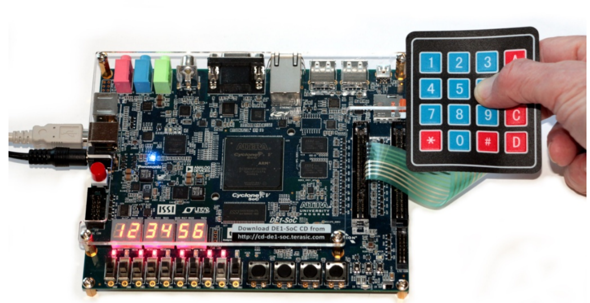
1. Digital logic devices.



2. Hex adding machine.



3. Keypad scanner.



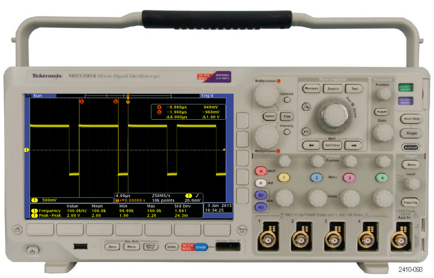
4. Keypad debouncer.

The first lab is a traditional EE lab assignment that will ask you to use our lab instruments to discover some basic electrical properties of real TTL logic devices, e.g., that they have propagation times and switching thresholds, verify their Boolean functions and prepare a proper report.

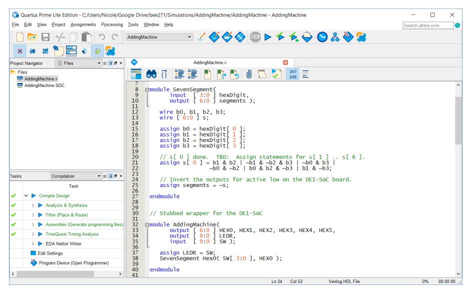
The remaining assignments are design projects using Verilog and our new Terasic DE1-SoC (system on a chip) FPGA boards. Lab 2 asks that you build a hex adding machine. (9 + 7 = 10 in hex.) Labs 3 and 4 ask that you build and demo a keypad scanner and debouncer in two stages, first the scanner, then the debouncer.

Group exercises

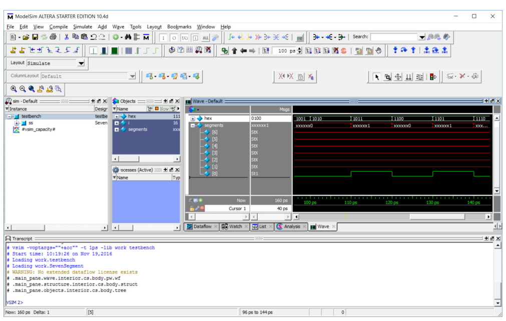
We will also do four group exercises in the lab, going through them together, step-by-step.



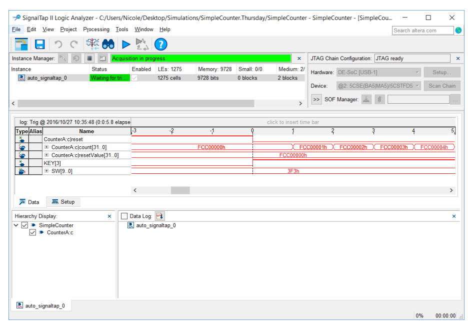
1. Using the lab instruments.



2. Creating and running a new Verilog project using Quartus.



3. Using the ModelSim simulator.



4. Using the SignalTap II logic analyzer.

Teams of 2

Students are expected to work in teams of two. No exceptions. It is up to you to select your partner. Realistically, this is an important choice.

You are expected to contribute equally on *every* lab. You can break up the tasks on any given lab any way you like. But you may not trade off entire labs, one of you doing all the work on one lab, the other doing all the work on the next. If your name is on the report, you must have contributed to it equally.

Because you are expected to contribute equally, you'll both get the same grade. If you find that your partner is not doing his or her share, your options are to try to work it out, swap for a more compatible partner or suck it up. I am not here to settle disputes between lab partners.

Submissions

I use Canvas to post materials and for submissions. Each team should submit *only one* copy of each submission but with both names on it. I do not like discovering that I'm grading the same report twice. To turn off the warning from canvas, you may submit an otherwise blank sheet saying only that your partner is submitting.

Reports

Only lab 1 requires a formal lab report, but it must be typed or handwritten neatly *in ink* and submitted as a PDF. I will not accept cellphone photographs of your work; they're simply too hard to read. If you submit a scan, it must have been made on an actual scanner. There are scanners available for student use in the UWB library in the Information Commons on the first floor. Microsoft Word and other formats can be converted to PDF for free at PDFOnline.com.

Please organize the material in your reports in the *same order* as in the assignment and *numbered the same*. I'll be reading them onscreen, so it's not helpful to paste things onto the end as appendices or send me hunting for Figure 3 unless it's on the same page. If you're submitting handwritten material, please do not try to squeeze everything onto one page.

I already have a copy of the assignment, so I do not need you to copy-and-paste it into your report. I also do not need title pages with colorful backgrounds, boxes identifying who did what, a list of the standard lab instruments at each bench or any conclusions not called for in the assignment.

I do need you to identify which part of the assignment you're answering and to include a schematic of *each* circuit being discussed. If you change a wire or a part, I need a new schematic.

Design projects

Labs 2 through 4 are design projects. On the design projects, I'll treat you the way any first line manager would on any similar design project: I'll ask that you demo your work and submit your code (your .v or .sv file) when you're done, then you'll start the next assignment. In lab 2, you'll also be asked to submit your Karnaugh maps as PDFs.

Grading

Realistically, I'm a hard grader on lab reports and an easy grader on design projects.

On lab reports, my objective isn't to be difficult but to improve your lab skills. My job is to go over your work to find absolutely everything about your procedure or your use of the lab instruments or your analysis that wasn't quite right and tell you, so you'll know how to do it better next time.

On the design projects, it is pretty much all about creating something, making it work and successfully demoing your design. I'll help you when you're stuck and at the end, I'll critique your designs and give you feedback on your coding. It's possible I might take off a few points for unnecessary ugliness in your code, but unlikely. If you created it yourself and you made it work and you experienced the satisfaction of that achievement, that's pretty much all I care about and that usually earns 100. If don't finish an assignment, submit what you have for partial credit.

Late policy in the lab

In the lab, I care far more about the quality of your work than about due dates. I realize it can be impossible to say how long debug will take before you find that last bug. So I tend to be forgiving of late lab assignments. But once I post grades (which usually takes a week, sometimes more), if you still weren't there, it's a zero. If you submit after grades have been posted, I will usually accept it for regrading without penalty. But I will never accept late submissions for regrading after the last day of instruction. *Except to correct a mistake, any grades posted during finals week really are final.*

All the work must be your own

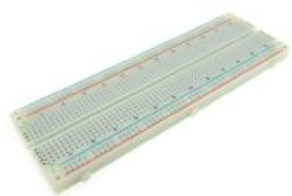
You may certainly compare notes with other teams and of course I understand that you may do research using Google. But absolutely everything you turn in to me must be your own work.

Copying answers from another student or off the internet will get a zero, even if you're clear about where you got them. If you omit the attribution, submit work that's not your own or try to deceive me with fabricated results, you will, in addition, *both* be reported for academic misconduct. If there are two names on the report, you're both responsible. I'm good at spotting misconduct and very good at reporting it. I do not give warnings and I do not accept excuses. I report everything.

Come prepared

To get the most out of the labs, you should read them before you arrive but this is a first EE class for many of you and there's no expectation that you arrive with any previous experience in our lab. You do not need to buy or bring anything except a notebook, a USB thumb drive and (optionally) your laptop. You will get a parts kit that includes everything else you need.

Parts kit



830-point (full-size) breadboard

Precut and preformed breadboard jumper wires

16-key numerical keypad

3-piece 20 cm multicolored 40-pin jumper wire "Dupont" ribbon cable set

Texas Instruments SN7400N Quad NAND or equivalent.

Texas Instruments SN7402N Quad NOR or equivalent.

Texas Instruments SN7404N Hex Inverter or equivalent.

Texas Instruments SN74LS86AN Quad XOR or equivalent.

3 Generic 470 ohm, 1/4 watt, 5% resistors

4 Generic 10K ohm, 1/4 watt, 5% resistors

3 Generic red LEDs

Disability

Access and Accommodations: Your experience in this class is important to me and to the University of Washington Bothell, where it is our policy and practice to create inclusive and accessible learning environments consistent with federal and state law.

If you experience barriers based on a temporary or permanent disability (including, but not limited to mental health, attention-related, learning, vision, hearing, physical or health impacts), please seek a meeting with Disability Resources for Students (DRS). They'll work with you and me and your other instructors to figure out some reasonable accommodations. The contact person is Rosa Lundborg at 425-352-5307 or email rlundborg@uwb.edu.

If you have already established accommodations with DRS, please tell me what they are so I can be sure to provide them.